AMENDMENTS TO THE CLAIMS

1.(currently amended): A turbo decoder for iteratively ~~performing decoding using results obtained by~~ decoding a received signal~~, and subsequently repeating decoding~~ a set number of times ~~using results of decoding obtained successively~~ comprising:

an error detector for detecting errors in results of decoding in parallel with a decoding operation; and

a controller which, when absence of error has been detected, is operable for outputting results of decoding and halting the decoding operation even if number of times decoding has been performed has not attained said set number of times.

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2.(original): A turbo decoder according to claim 1, wherein said controller monitors the number of times errors are detected in decoded results when decoding has been performed said set number of times and executes the decoding operation further if the number of times errors are detected is equal to or less than the set value.

3.(cancelled)

4.(currently amended): A turbo decoder for receiving first data, second data obtained by encoding said first data, and third data obtained by interleaving and then encoding said first data, as signals ya, yb and yc, respectively, and executing decoding processing repeatedly using these received signals, comprising:

first and second elementary decoders for executing second decoding processing using results of ~~decoding, which are obtained by~~ applying first decoding processing to ~~prescribed~~ received signals ya[[,]] and yc, and also using ~~the other~~ received signal yb, and subsequently executing, repeatedly, first decoding processing using ~~second~~ results of second decoding processing and also using said received [[signals ya,]] signal yc, and second decoding processing using ~~first~~ results of first decoding processing and also using said ~~other~~ received signal yb;

an interleaving unit for interleaving the received signal ya and the ~~second~~ results of the second decoding processing and inputting the same to the first elementary decoder ~~together with the received signal yc~~; and

a deinterleaving unit for deinterleaving the ~~first~~ results of the first decoding processing and inputting the same to the second elementary decoder ~~together with the received signal yb~~;

wherein results of final decoding processing are output from said second elementary decoder directly without intervention of interleaving or deinterleaving.

5.(currently amended): A turbo decoder for receiving first data, second data obtained by encoding said first data, and third data obtained by interleaving and then encoding said first data, as signals ya, yb and yc, respectively, and executing decoding processing repeatedly using these received signals, comprising:

one elementary decoder for executing second decoding processing using results of ~~decoding, which are obtained by~~ applying first decoding processing to [[a]] received ~~signal~~ signals ya and yc, and ~~another~~ also using received signal yb, and subsequently executing,

repeatedly, first decoding processing using ~~second~~ results of second decoding processing and also using said received signal yc; and second decoding processing using ~~first~~ results of first decoding processing and also using said ~~other~~ received signal yb;

an interleaving unit for interleaving the received signal ya and inputting the same to the elementary decoder;

a selection circuit for selecting the signal yc when the first decoding processing is executed, selecting the signal yb when the second decoding processing is executed, and inputting the selected signal to the elementary decoder; and

means for deinterleaving results of the first decoding processing, interleaving results of the second decoding processing and inputting the deinterleaved and interleaved results to the elementary decoder; wherein results of decoding are output from said elementary decoder directly without intervention of interleaving or deinterleaving.

6.(currently amended): A turbo decoder for iteratively ~~performing decoding using results obtained by~~ decoding a received signal~~, and subsequently repeating decoding~~ a set number of times ~~using results of decoding obtained successively~~, comprising:

first and second elementary decoders for executing second decoding processing using results of ~~decoding, which are obtained by~~ applying first decoding processing to a prescribed received signal, and also using another received signal, and subsequently executing, repeatedly, first decoding processing using ~~second~~ results of second decoding processing and also using said prescribed received signal, and second decoding processing using ~~first~~ results of first decoding processing and also using said other received signal; and

a selection circuit for selecting and outputting the ~~first and second~~ results of first and second decoding processing output from said first and second elementary decoders;

wherein the nature of an error generation pattern in decoded data finally output is controlled by selecting the decoded data to be output.

7.(currently amended): A turbo decoder for iteratively ~~performing decoding using results obtained by~~ decoding a received signal~~, and subsequently repeating decoding~~ a set number of times ~~using results of decoding obtained successively~~ comprising:

first and second elementary decoders for executing second decoding processing using results of ~~decoding, which are obtained by~~ applying first decoding processing to a first received signal, and also using another received signal, and subsequently executing, repeatedly, first decoding processing using ~~second~~ results of second decoding processing and also using said first received signal, and second decoding processing using ~~first~~ results of first decoding processing and also using said other received signal; and

a selection circuit for selecting a combination of received signals, input to the first elementary decoder that executes said first decoding processing and selecting a received signal input to the second elementary decoder that executes the second decoding processing;

wherein the nature of an error generation pattern in decoded data is controlled by switching the received signals input to the first and second elementary decoders.

8.(currently amended): A turbo decoder for iteratively ~~performing decoding using results obtained by~~ decoding a received signal~~, and subsequently repeating decoding~~ a set number of times ~~using results of decoding obtained successively~~ comprising:

one elementary decoder for executing second decoding processing using results of ~~decoding, which are obtained by~~ applying first decoding processing to a received signal, and also using another received signal, and subsequently executing, repeatedly, first decoding processing using ~~second~~ results of second decoding processing and also using said received signal, and second decoding processing using ~~first~~ results of first decoding processing and also using said other received signal; and

a selection circuit for selecting a combination of received signals input to the elementary decoder at a timing at which said first decoding processing is executed, and selecting a received signal input to the elementary decoder at a timing at which said second decoding processing is executed;

wherein the nature of an error generation pattern in decoded data is controlled by switching the received signals input to the elementary decoder at the timings of the first and second decoding processing.

9.(new): A turbo decoder for iteratively decoding a received signal, comprising:

an error detector for detecting errors in results of previous decoding in parallel with a current decoding operation in the iterative decoding processing; and

a controller which, when absence of error has been detected, is operable for outputting results of decoding and halting the decoding operation even if a number of times decoding has been performed has not attained a set number of times.

10.(new): A turbo decoder for executing first decoding processing using a first set of signals including a first received signal selected from among received signals, and executing

second decoding processing using a second set of signals including a second received signal selected from among the received signals, comprising:

an error detector for detecting errors in results of one decoding processing while other decoding processing is being executed.

11.(new): A turbo decoder for executing first decoding processing using a first set of signals including a first received signal selected from among received signals, and executing second decoding processing using the results of the first decoding processing and a second set of signals including a second received signal selected from among the received signals, comprising:

a memory for storing the results of the first decoding processing;

an error detector for detecting errors in the results of the first decoding processing; and

means for outputting the results of the first decoding processing stored in said memory in accordance with the result of the error detection.

12.(new): The turbo decoder according to claim 11, wherein said memory stores the results of the first and second decoding processing alternatively.

13.(new): The turbo decoder according to claim 11, wherein a signal obtained by interleaving the results of the first decoding processing is used for the second decoding processing.

14.(new): A turbo decoder for executing first decoding processing using a first set of signals including a first received signal selected from among received signals, and executing second decoding processing using a second set of signals including a second received signal selected from among the received signals, comprising:

a decoder for executing the first and second decoding processing and executing the second decoding processing using a signal obtained by interleaving the results of the first decoding processing; and

a controller for controlling the decoder so that the first decoding processing is executed and then the second decoding processing is executed.

15.(new): A turbo decoder for executing first decoding processing using a first set of signals including a first received signal selected from among received signals, and executing second decoding processing using a second set of signals including a second received signal selected from among the received signals, comprising:

a decoder for executing the first and second decoding processing and executing the second decoding processing using a signal obtained by interleaving the results of the first decoding processing; and

an output line for outputting a signal obtained by deinterleaving the results of the second decoding processing as a decoding result of the turbo decoder.

16.(new): A turbo decoder for executing first decoding processing using a first set of signals including a first received signal selected from among received signals, and executing

second decoding processing using a second set of signals including a second received signal selected from among the received signals, comprising:

a decoder for executing the first and second decoding processing and executing the second decoding processing using a signal obtained by deinterleaving the results of the first decoding processing; and

output means for outputting the results of decoding processing in the decoder directly without intervention of interleaving or deinterleaving.

17.(new): A turbo decoder for executing first decoding processing using a first set of signals including a first received signal selected from among received signals, and executing second decoding processing using a second set of signals including a second received signal selected from among the received signals, comprising:

a selector for selecting and outputting one of the results of the first and second decoding processing.

18.(new): A turbo decoder according to claim 17, wherein in a case where the second decoding processing is executed using a signal obtained by interleaving the results of the first decoding processing, said selector selects and outputs a signal obtained by deinterleaving the results of the second decoding processing as a decoding output of the turbo decoder.

19.(new): A turbo decoder according to claim 17, wherein in a case where the second decoding processing is executed using a signal obtained by interleaving the results of the first

decoding processing, said selector selects and outputs the results of the first decoding processing directly without intervention of interleaving or deinterleaving.

20.(new): A turbo decoder for executing first decoding processing using a first set of signals including a first received signal selected from among received signals, and executing second decoding processing using a second set of signals including a second received signal selected from among the received signals, comprising:

a controller for changing an order of the first and second decoding processing, between a first and a second order, wherein the first decoding processing is executed and then the second decoding processing is executed in the first order, and the second decoding processing is executed and then the first decoding processing is executed in the second order.

21.(new): A turbo decoder for executing first decoding processing using a first set of signals including a first received signal selected from among received signals, and executing second decoding processing using a second set of signals including a second received signal selected from among the received signals, comprising:

a decoder for executing the first and second decoding processing; and

a controller for changing an order of the first and second decoding processing, between a first and a second order, wherein the first decoding processing is executed and then the second decoding processing is executed in the first order, and the second decoding processing is executed and then the first decoding processing is executed in the second order.

22.(new): A turbo decoder for executing first decoding processing using a first set of signals including a first received signal selected from among received signals, and executing second decoding processing using a second set of signals including a second received signal selected from among the received signals, comprising:

a decoder for executing the first and second decoding processing; and

a controller for outputting selectively one of the results of the first and second decoding processing as the output of the turbo decoder.

23.(new): A turbo decoder for executing first decoding processing using a first set of signals including a first received signal selected from among received signals, and executing second decoding processing using a second set of signals including a second received signal selected from among the received signals, comprising:

a controller for controlling decoding processing so that the second decoding processing is executed using a signal obtained by deinterleaving the results of the first decoding processing in a case where the turbo decoder executes decoding processing for each unit of the units of turbo code consisted of a plurality of information blocks.